REMARKS/ARGUMENTS

In this amendment, claims 6 and 9 are amended. Claim 6 is rewritten in independent form and claim 9 is amended to correct a typographical error. Claims 1-4 were previously cancelled without prejudice. Claims 5-9 remain pending. Applicants' attorney expresses appreciation to Examiner Chow for discussing this application on April 26, 2006. The invention described in paragraph [0016] of the specification and illustrated in Fig. 2 was discussed. Claims 9, 5 and 6 and the cited prior art patents, Poirion and Kang, were discussed. Examiner Chow asked Applicants to submit a written response to the Office Action for his consideration.

Applicants respectfully submit that currently pending claims 5-9 would not have been obvious from the combined teachings of Poirion and Kang and request favorable reconsideration in view of the following arguments

Claim Rejections – 35 USC § 103. Claims 5-9 were rejected under Section 103(a) as being unpatentable over Poirion in view of Kang.

Regarding Claims 5-8

Claim 5 recites a core logic chip incorporating two memory control circuits: a primary memory control circuit and a backup memory control circuit. Both memory control circuits are controlled by the graphics accelerator to assert first and second read/write signals, respectively. Claim 5 further recites first and second data transmission channels that transmit the first and second read/write signals, respectively, to the system memory. Each of the first and second read/write signals is part of a specific read/write signal "for obtaining a specified image data from said system memory to be processed by said graphics accelerator." Claim 6 recites the features of claim 5 and specifies that the system memory includes a frame buffer "where said image data is stored."

Poirion in view of Kang fails to disclose that each of said first and said second read/write signals is a part of a specific read/write signal for obtaining a specified image data from said system memory to be processed by said graphics accelerator. **According to the present invention, the specified image data in the system memory is obtained by the graphics accelerator via at least two paths**, i.e. the first and second data transmission channels. In

contrast, in Poirion, the graphics controller 5 (that is considered equivalent to the graphics accelerator of the present invention by the Examiner) accesses the frame buffer 18 through the frame buffer controller 15 (that is considered equivalent to the backup memory control circuit of the present invention by the Examiner) and the frame buffer bus 17 (that is considered equivalent to the second data transmission channel of the present invention by the Examiner). Poirion's image data in the frame buffer is only accessed via the frame buffer bus 17, which is only one data transmission channel. Poirion's Fig. 2 clearly illustrates that the graphics controller accesses image data in the frame buffer via the frame buffer controller 15 and the frame buffer bus 17. Poirion's graphics controller does not access image data in the frame buffer via the memory controller 4, system bus 10, and system memory 9. Even if the system memory contains the frame buffer, Poirion does not disclose or suggest accessing image data in the frame buffer via two data transmission channels. As discussed above, specified image data according to claim 5 is accessed via two data transmission channels.

Poirion teaches that the graphics controller need not share the system memory 9 with the processor, thus avoiding the memory sharing problems (col. 3, lines 57-64). In this case, the memory controller 4 and system bus 10 are not used by the graphics controller 5. If the frame buffer 18 is not present (Fig. 1), the memory controller 4 and system bus 10 are used by the graphics controller 5 (col. 3, lines 50-56). Basically, **only one path is used by the graphics accelerator according to Poirion**, which is quite different from the present invention. Even though the access of the graphics controller to the system memory may be arranged to be available in Poirion (col. 3, lines 65-67), there is no teaching or suggestion that Poirion's graphics accelerator uses both the system bus 10 and frame buffer bus 17 to obtain "a specified image data" as recited in claims 5-8. Moreover, there is no teaching or suggestion of an object of the present invention, i.e. the bandwidth enhancement for data transmission between the graphics accelerator and the system memory.

The Kang patent was cited for the purpose of disclosing system memory that contains a frame buffer. Kang fails to disclose those features of the invention which are not disclosed by Poirion. In view of the foregoing, Applicants respectfully submit that claims 5-8 would not have

been obvious from the combined teachings of Poirion and Kang. Withdrawal of the rejection is respectfully requested.

Regarding claim 9

Claim 9 is similar to claim 6 and recites that both the primary memory control circuit and backup memory control circuit are coupled to the graphics accelerator and "accessible to a frame buffer in said system memory at a request of said graphics accelerator." Claim 9 further recites that the first and second data transmission channels transmit portions of the image data from the frame buffer in response to the first and second read/write signals.

Poirion in view of Kang fails to disclose that the first and second data transmission channels transmit first and second portions of an image data from the frame buffer in the system memory in response to first and second read/write signals issued by the primary memory control circuit and the backup memory control circuit, respectively. According to Poirion, it is intended to use the single-chip chipset in either the configuration with a separate frame buffer or the configuration without a separate frame buffer. In the configuration with a separate frame buffer 18, the graphics controller 5 accesses the frame buffer 18 through the frame buffer controller 15 and the frame buffer bus 17 (col. 3, lines 57-64; Fig. 2). On the other hand, in the configuration without a separate frame buffer 18, i.e. the frame buffer is disposed in the system memory, the graphic controller 15 accesses the shared system memory 9 through the memory controller 4 and the system bus 10, and the frame buffer controller 15 is not used (col. 3, lines 50-56; Fig. 1). Poirion does not disclose or suggest accessing image data in the frame buffer via both a primary memory control circuit and first data transmission channel and a backup memory control circuit and second data transmission channel as recited in claim 9. In other words, **in Poirion's configuration disclosing a frame buffer, image data in the frame buffer is only accessed via the frame buffer controller 15 and frame buffer bus 17**. Poirion's graphics accelerator uses only one path to access image data from the frame buffer.

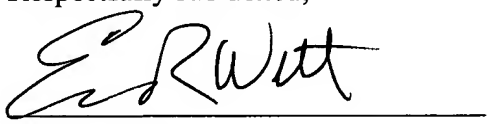
In contrast, claim 9 recites both the primary memory control circuit and backup memory control circuit are coupled to the graphics accelerator and "accessible to a frame buffer in said system memory at a request of said graphics accelerator." There is no such teaching or

suggestion in Poirion. Claim 9 further recites that the first and second data transmission channels transmit portions of the image data from the frame buffer in response to the first and second read/write signals. Again, Poirion does not teach or suggest transmitting portions of the image data via two data transmission channels.

In view of the foregoing, Applicants submit that claim 9 would not have been obvious from the combined teachings of Poirion and Kang. Withdrawal of the rejection is requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If there are any remaining issues preventing allowance of the pending claims that may be clarified by telephone, the Examiner is requested to call the undersigned.

Respectfully submitted,



Evan R. Witt
Reg. No. 32,512
Attorney for Applicants

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MADSON & AUSTIN
Gateway Tower West
15 West South Temple, Suite 900
Salt Lake City, Utah 84101
Telephone: 801/537-1700